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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,923	10/27/2003	Michael M. Klock	NVID-062/00US 140060-2128	5104
23419 7590 12/27/2007 COOLEY GODWARD KRONISH LLP ATTN: Patent Group Suite 1100 777 - 6th Street, NW Washington, DC 20001			EXAMINER WASHBURN, DANIEL C	
			ART UNIT 2628	PAPER NUMBER
			MAIL DATE 12/27/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	10/694,923		KLOCK ET AL.	
	Examiner		Art Unit	
	Dan Washburn		2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,7,8,21,25 and 28-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,7,8,21,25 and 28-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/25/07 has been entered.

Response to Arguments

Applicant's arguments filed 10/25/07 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., measuring processor utilization) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claims recite measuring an attribute that is indicative of utilization of a graphics processor, but this is not considered the same as directly measuring graphics processor utilization. The examiner's arguments presented below are directed at the notion that Giemborek doesn't describe measuring an attribute that is indicative of processor utilization, as this is within the scope of the rejected claims.

As to the applicant's argument that Giemborek doesn't measure an attribute that is indicative of processor utilization, the examiner contests that Giemborek describes that power conservation in the graphics accelerator is achieved, without sacrificing graphics processing, by matching the speeds of adjustable clocks so as to provide only the processing power required. The clock sources 40 and 42 (see Figure 1) in the graphics accelerator are programmable so as to match their speed to processing requirements (column 4 lines 64-67 through column 5 lines 1-5). Thus, the processing requirements (which are attributes that determine the level of processor utilization) are measured and these requirements are used to adjust the clocks sent to the processors such that the required processing power is provided.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Giemborek describes adjusting the clock rate of processors within a system based on the measured utilization of the processors, for the purpose of reducing the power consumed by the system (column 1 lines 50-65). Williams describes adjusting the clock rate of one or more processors within a system based on the measured utilization of the one or more processors, for the purpose of increasing the average clock rate of the processors while

not overheating and causing damage to system components (column 6 lines 13-50).

Thus, while the two inventions are intended to solve different problems, they are considered analogous art because they both measure the utilization of a processor and adjust the rate of the clock signal sent to that processor according to the measured utilization. See the rejection of claims 1 and 21 for the rationale used to combine Giemborek with Williams.

As to the applicant's argument that the cited art does not describe discrete performance levels further in which, "the selected performance level being a minimum performance level sufficient to maintain the display rate within a normal range," the examiner contests that Giemborek at column 1 lines 50-65 explicitly describes that the clock speeds (each clock speed is considered a discrete performance level) sent to the graphics accelerator are matched to the actual graphics display requirements to ensure that display performance is not sacrificed, which is considered discrete performance levels further in which the selected performance level being a minimum performance level sufficient to maintain the display rate within a normal range.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Giemborek et al. (US 6,950,105).

As to claim 25, Giemborek describes a graphics system, comprising:

a graphics processor having a sequence of at least two discrete performance levels where each performance level is defined by a graphics processor core clock rate of a graphics processing unit and a memory clock rate (column 1 lines 50-67 through column 2 lines 1-11 and Figure 1 describes graphics accelerator 10, which matches the speed of at least one of two or more clocks (e.g., engine clock 40 and memory clock 42) to levels (speeds) under software control to a rate sufficient to satisfy current display requirements. The graphics accelerator includes 2D/3D engine 20, overlay engine 22, and frame buffer 16);

a graphics memory coupled to said graphics processor by a graphics bus and operable at said memory clock rate (Figure 1 and column 2 lines 27-36 describes frame buffer memory 16);

a performance level controller, said performance level controller configured to monitor, as function of time, at least one attribute of said graphics system indicative of a level of utilization of at least one component of said graphics system for which over-utilization of said component decreases a display rate (column 5 lines 21-48 and column 7 lines 5-49 describes that the CPU 12 determines the required graphics processing based on the software running on the CPU 12 and various display mode settings of the computer. The CPU 12 uses this information to calculate the frame buffer access bandwidth requirement and then adjusts the clock speeds of clocks 40 and 42 until the clock speeds are sufficiently fast to meet the frame buffer access bandwidth requirement, which conserves the battery power of the portable device without sacrificing graphics display performance (column 1 lines 50-65)), and

said performance level controller configured to increase said performance level to avoid over-utilization of said at least component (column 7 lines 50-67 through column 8 lines 1-2 describes increasing the clock speeds of clocks 40 and 42 if the required bandwidth is higher than the available bandwidth required by the initially-chosen clock speed);

said performance level controller configured to decrease said performance level from a high performance level to a lower performance level to avoid under-utilization of said at least one component (column 8 lines 16-27 describes that clock speeds of clocks 40 and 42 are reduced if the required bandwidth is less than the available bandwidth provided by the revised clock speeds);

the graphics system operating at the core clock rate and memory clock rate associated with the performance level selected by the performance level controller, the selected performance level being a minimum performance level capable of maintaining the display rate within a normal range (column 1 lines 50-65 describes that the clock speeds are selected to ensure that the graphics display performance is not degraded).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giemborek et al. (US 6,950,105) in view of Williams et al. (US 6,397,343).

As to claim 1, Giemborek describes a method of operating a graphics system having a sequence of at least two discrete performance levels with each performance level being defined by a core clock rate of a graphics processing unit and a memory clock rate, the method comprising:

monitoring a first attribute indicative of utilization of a graphics engine within a graphics processor core clock domain and determining whether the graphic engine is under-utilized or over-utilized (column 5 lines 21-48 describes that clock speeds of the clocks on the graphics accelerator 10 are chosen based on the required graphics processing. The required graphics processing is determined by factors that include the

software running on the CPU 12 and various display mode settings, including screen resolution, pixel or color depth, and screen refresh rate);

monitoring a second attribute indicative of utilization of a graphics memory within a graphics memory clock domain and determining whether the graphics memory is under-utilized or over-utilized (column 5 lines 21-48 describes that clock speeds of the clocks on the graphics accelerator 10 are chosen based on the required graphics processing. The required graphics processing is determined by factors that include the software running on the CPU 12 and various display mode settings, including screen resolution, pixel or color depth, and screen refresh rate);

selecting a performance level to maintain a display rate within a normal range by increasing the performance level in response to detecting an over-utilization condition and decreasing the performance level in response to detecting an under-utilization condition (column 7 lines 50-67 through column 8 lines 1-27 describes increasing the clock speeds of the clocks within the graphics accelerator 10 if the system is currently over-utilized and decreasing the clock speeds of the clocks within the graphics accelerator 10 if the system is currently under-utilized. Column 1 lines 50-65 describes that the clock speeds are set such that display rate remains in a normal range (i.e., graphics display performance is not sacrificed)); and

operating the graphics system at the core clock rate and memory clock rate associated with the selected performance level, the selected performance level being a minimum performance level sufficient to maintain the display rate within the normal

range (column 1 lines 50-65 describes that the clock speeds are set such that display rate remains in a normal range (i.e., graphics display performance is not sacrificed)).

Giemborek doesn't describe that monitoring the first attribute includes monitoring an attribute indicative of utilization of a graphics pipeline within a graphics processor core clock domain and determining whether the graphic pipeline is under-utilized or over-utilized.

However, Williams describes a method and system that includes a device for dynamic graphics subsystem clock adjustment within a computer system having a CPU and a dedicated graphics subsystem. A system interface is coupled to the graphics subsystem to allow a controller to determine the graphics processing load placed on the graphics subsystem (column 4 lines 11-31 and column 6 lines 33-50). Williams further describes that monitoring said at least one attribute (in this case the graphics processing load placed on the graphics subsystem) comprises: monitoring at least one attribute indicative of utilization of a graphics pipeline within a graphics processor core clock domain and determining whether the graphic pipeline is under-utilized or over-utilized (column 6 lines 51-67, column 7 lines 1-20, and column 8 lines 11-22 describes that the device 100 determines the graphics subsystem load by monitoring the processing activity of graphics subsystem 200 via the pipeline control 206 (e.g., by snooping graphics commands and data flowing through a graphics pipeline to determine the activity level of the graphics pipeline) and adjusts the pipeline clock frequency accordingly).

All the limitations of claim 1 are known in Giemborek and Williams, the only difference is the combination of old elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Giemborek the system and method of determining the processing load placed on a graphics subsystem by monitoring the level of activity of a graphics pipeline, and adjusting the frequency of the pipeline clock according to the determined load, as taught by Williams, as this doesn't change the operation of the rest of the system, and it could be used to achieve the predictable results of improving the efficiency of the 2D/3D graphics engine disclosed in Giemborek by monitoring the pipeline activity within the graphics engine and determining a required clock rate to be passed to the engine based, in part, on the monitored activity. One advantage of passing the graphics engines a variable clock rate based at least in part on calculated activity within a pipeline within the engine is that the system can further reduce its power consumption and optimize its calculated clock rates by adding the activity of the pipeline to the list of factors that are used when determining the clock rates.

Concerning claim 21, Giemborek describes a method of operating a graphics system having a sequence of at least two discrete performance levels where each performance level is defined by a core clock rate of a graphics processing unit and a memory clock rate, the performance levels including a high performance level for processing complex three-dimensional graphical images and at least one lower power, lower performance level for processing less complex graphical images, the method comprising:

monitoring as a function of time attributes of a graphics engine and a graphics memory of said graphics system that are indicative of a level of utilization of said graphics system (column 5 lines 20-48 describes that the system monitors a set of factors that are used to determine the required graphics processing load (and thus, the required clock speeds of the clocks within the graphics accelerator). The factors include the software running on the host CPU, as well as display mode settings of the computer. Column 7 lines 36-67 through column 8 lines 1-27 specifically describes the process that the system follows when monitoring the graphics processing load placed on the graphics accelerator);

in response to detecting a level of utilization greater than an over-utilization threshold for which a display rate of the graphics system is likely to be significantly decreased below a normal display rate, selecting a higher performance level (column 7 lines 50-67 and column 1 lines 50-65); and

in response to detecting a level of utilization below an under-utilization threshold, selecting a lower performance level to reduce power required by the graphics system (column 8 lines 16-27); and

operating the graphics system at the core clock rate and memory clock rate associated with the selected performance level, the selected performance level being a minimum performance level sufficient to maintain the display rate within the normal range (column 1 lines 50-65).

Giemborek doesn't describe that monitoring the first attribute includes monitoring an attribute indicative of utilization of a graphics pipeline within said graphics system.

However, Williams describes monitoring an attribute indicative of utilization of a graphics pipeline within a graphics system (see the rejection of claim 1).

See the rejection of claim 1 for the rationale used to combine Williams with Giemborek, as the same rationale applies here.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giemborek in view of Williams as applied to claim 1 above, and further in view of Bose et al. (US 7,076,681).

Regarding claim 7, Giemborek in view of Williams doesn't describe monitoring the percentage of clock cycles in a graphics pipeline for which said at least one stage is held up waiting for the results of another stage.

However, Bose describes an integrated circuit such as a scalar processor. Circuit components or units are clocked by and synchronized to a common system clock. A local clock generator in each clocked unit combines the common system clock and stall status from one or more other units to adjust the register clock frequency up or down (column 3 lines 52-62). Bose further describes (column 6 lines 36-60 and Figure 2) an example that includes an instruction unit (I-unit) and an execution unit (E-unit), the I-unit and E-unit include activity monitoring and clock control logic 126, 128, respectively, which monitor unit activity level. When the E-unit 124 senses a stall condition it asserts a stall bit 130, which is used to adjust down the clock speed of the I-unit clock (to throttle down the I-unit and effectively reduce the instruction rate to the E-unit). Depending on the granularity of the control the E-unit activity status or stall bit 130 can adjust its own clock within the E-unit. When the E-unit stall ends the I-unit clock is

throttled back up to its normal clock rate. Similarly, when the I-unit experiences a stall condition it sends an I-pipe empty bit to the E-unit so the E-unit can adjust down its clock to conserve power. The activity monitoring and clock control logic 126, 128 contained within each stage of the scalar processor is considered to monitor the percentage of clock cycles in a graphics pipeline for which at least one stage (e.g., the E-unit) is held up waiting for the result of another stage (e.g., the I-unit). In this case when the percentage of clock cycles for which the E-unit is held up waiting for the results of the I-unit is greater than zero the activity monitoring and clock control logic within the I-unit notifies the E-unit stage to reduce its clock speed in order to conserve power until the stalling I-unit overcomes the stall.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Giemborek in view of Williams the system and method of monitoring the percentage of clock cycles in a graphics pipeline for which at least one stage is held up waiting for the results of another stage, as taught by Bose, in order to achieve the predictable result of improving the efficiency and power conservation of the 2D/3D graphics engine (disclosed in Giemborek) by monitoring the pipeline activity within the graphics engine and determining a clock rate for each stage within the pipeline. The advantage of assigning a clock rate to each stage within the pipeline, rather than simply passing them a single clock rate, is that the system can further reduce its power consumption by adjusting the clock rate of stages that are waiting for the results of another stage in order to conserve power at those stage until the stalling stage produces its result.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giemborek in view of Williams as applied to claim 1 above, and further in view of Jun et al. (US 6,112,310).

With regard to claim 8, Giemborek describes determining if the current frame buffer access bandwidth is high enough to at least meet the calculated required access bandwidth of the frame buffer (column 7 lines 19-49). But Giemborek in view of Williams doesn't describe monitoring the percentage of clock cycles in a graphics memory for which a memory bandwidth of said graphics memory is inadequate.

However, Jun describes a system and method wherein the percentage of bus cycles that are also memory access cycles is calculated and the frequency of the memory clock is adjusted up or down according to the calculation (column 4 lines 5-49 and column 5 lines 6-23), which is considered monitoring the percentage of clock cycles in a graphics memory for which a memory bandwidth of said graphics memory is inadequate (or more than adequate, as the case may be), and adjusting the frequency of the memory clock accordingly.

All the limitations of claim 8 are known in Giemborek, Williams, and Jun, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Giemborek and Williams the system and method of monitoring the percentage of clock cycles in a graphics memory for which a memory bandwidth of said graphics memory is inadequate, as taught by Jun, in order to achieve the predictable result of improving the efficiency of the frame buffer disclosed in

Giemborek by monitoring the frame buffer activity and determining a required clock rate to be passed to the frame buffer based, in part, on the monitored activity. One advantage of passing the frame buffer a variable clock rate based at least in part on calculated activity within the frame buffer is that the system can further reduce its power consumption and optimize its calculated clock rates by adding the activity of the frame buffer to the list of factors that are used when determining the clock rates.

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giemborek et al. (US 6,950,105) in view of Williams et al. (US 6,397,343), as applied to claims 1 and 21 above, and further in view of Culbert et al. (US 6,820,209).

As to claims 28 and 29, Giemborek describes a 2D/3D graphics engine that is capable of operating at different clock speeds (column 2 lines 42-67), where the 2D/3D graphics engine is operated at a speed that is determined based on factors that include the software running on a host CPU, as well as display mode settings of the computer, such as screen resolution, pixel or color depth, and screen refresh rate (column 5 lines 13-48).

Giemborek in view of Williams doesn't describe the method of claims 1 or 21, wherein said at least two discrete performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.

However, Culbert describes a system and method wherein at least two discrete performance levels include a low power two-dimensional graphics performance level, a

standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level (column 5 lines 46-67 through column 6 lines 1-43 describes a system that includes a 2D graphics engine 212 and a separate 3D graphics engine 214. The 2D and 3D graphics engines are only activated when the graphics controller needs to produce 2D or 3D graphics. Further, column 6 lines 44-67 through column 7 lines 1-16 describes that the graphics controller supplies a clock signal to the 2D engine and a second clock signal to the 3D engine. To reduce power consumption, the clock signal normally sent to the 2D engine is stopped when the 2D engine is not being utilized, and likewise the clock signal normally sent to the 3D engine is stopped when its processing resources are not being utilized. Thus, Culbert is considered to describe a low power two-dimensional graphics performance level (when the 2D processor isn't being utilized), a standard two-dimensional graphics performance level (when the 2D processor is being utilized), a low-power three-dimensional graphics performance level (when the 3D processor isn't being utilized), and a high performance three-dimensional graphics performance level (when the 3D processor is being utilized)).

All the elements of claims 28 and 29 are known in Giemborek, Williams, and Culbert, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Giemborek in view of Williams the system and method wherein said at least two discrete performance levels include a low power two-

dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level, as taught by Culbert, as a system and method wherein the 2D engine is separate from the 3D engine, and where each engine is separately controlled, could be used to achieve the predictable result of more effectively saving power, as when only the 2D or only the 3D engine is required for a particular operation, the other engine can be powered down, which doesn't degrade the performance of the system, and reduces power consumption even more than clocking the 2D and 3D engines up and down together (as described in Giemborek).

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giemborek et al. (US 6,950,105), as applied to claim 25 above, and further in view of Culbert et al. (US 6,820,209).

As to claim 30, Giemborek describes a 2D/3D graphics engine that is capable of operating at different clock speeds (column 2 lines 42-67), where the 2D/3D graphics engine is operated at a speed that is determined based on factors that include the software running on a host CPU, as well as display mode settings of the computer, such as screen resolution, pixel or color depth, and screen refresh rate (column 5 lines 13-48).

Giemborek doesn't describe the system of claim 25, wherein the performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics

performance level, and a high performance three-dimensional graphics performance level.

However, Culbert describes a system and method wherein the performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level, as described in the rejection of claims 28 and 29. See the rejection of claims 28 and 29 for a complete analysis of Culbert and for the rationale used to combine Culbert with Giemborek, as the same rationale applies here.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Washburn whose telephone number is (571) 272-5551. The examiner can normally be reached on Monday through Friday 8:30 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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12/17/07


ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER